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REMARKS

Claims 24-59 are pending in this application. Claims 24 and 48 are amended herein. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Claims 24-25, 33-36, 39-40, 45-52 and 55-57 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba (U.S. Patent No. 6,525,403).

Claims 26-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Park et al. (A 40nm body-tied Finfet (OMEGA MOSFET) using bulk Si wafer, Physica E 19 (2003), pages 6-12).

Claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Huang (U.S. Patent No. 5,893,741).

Claim 34 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Clark et al. (U.S. Patent No. 6,635,909).

Claims 37-38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Yu (U.S. Patent No. 6,342,410).

Claims 41 and 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Yu (U.S. Patent No. 6,475,890).

Claim 42 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Hu et al. (U.S. Patent No. 6,413,802).

Claim 43 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba in view of Muller et al. (U.S. Patent No. 6,432,829).

Claim 54 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, in view of Yu (U.S. Patent No. 6,342,410).

Claim 56 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, in view of Park.

As an initial note, the Office Action states in Office Action Summary that Claims 24-58 are pending. The Office Action does not mention Claim 59, which was added in the amendment dated September 24, 2003. Applicants respectfully request clarification as to the status of this claim. Applicants further note that final rejection of this claim is inappropriate.

Also, as an initial point for the discussion of Claim 24, the Office Action states that Figure 5 in Inaba "shows a masking layer (123) over the isolation region and covering a lower portion of the semiconductor fin." (Office Action, page 3). However, the layer referenced by 123 is actually an insulating film layer. (Inaba, Col. 2, Line 38). The masking layer is referenced by number 124 (Inaba, Col. 2, Line 40), and is only shown on Figure 4. Applicants have assumed that this is the masking layer to which the Office Action is referring. If this is in error, Applicants respectfully request clarification on this issue.

Claim 24 has been amended. In particular, Claim 24 now recites "after forming the gate electrode, forming a masking layer over the isolation region and covering a lower portion of the semiconductor fin; and forming a source region and a drain region in uncovered portions of the semiconductor fin, using the masking layer as a mask, the source region having a source-substrate junction and the drain region having a drain-substrate junction, the source-substrate junction or drain-substrate junction being higher than the bottom surface of the gate electrode by an amount based on a thickness of the masking layer." Applicants respectfully submit that the references of record do not teach or suggest the limitations of Claim 24. Inaba, in Figure 4, shows a mask layer 124 that is deposited and removed prior to the doping of the source and drain regions as shown in Figure 5. Because the prior art referenced in Inaba does not show the same

method as Applicants' present invention, Applicants' present invention cannot be an obvious modification under 35 U.S.C. 103 of the inventions disclosed in Inaba. Accordingly, Applicants respectfully request that the rejection of this Claim be withdrawn.

Claim 48 has been amended as set forth above to more particularly recite an embodiment of Applicants' invention. This amendment more clearly explains that "after etching portions of the gate electrode layer, forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material; and after forming the region of material, doping the sidewall of the semiconductor fin above the region of material." Inaba simply does not teach or suggest the required process steps in the required order. In Inaba's Figure 5, there is no suggestion to first form a gate electrode, then form a region of material, and then dope a sidewall above the region of material. Rather, in Inaba's Figure 5 the masking region 124 is removed prior to forming source/drain regions 126. Accordingly, Applicants respectfully request that the rejection of this Claim be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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